REMARKS

The Applicant sincerely appreciates the Examiner's thorough examination of the present application as evidenced by the Office Action of June 14, 2006 ("the Office Action"). As discussed in greater detail below, the Applicant has amended Claims 1-4, 6-7, 9-19, 21-27, 29-31, 33-40, 42-52, 55, and 57; added new Claims 63-79; and canceled Claims 20, 41, and 53-54. The Applicant will also show in the following remarks that all claims are patentable over the cited art.

Accordingly, the Applicant respectfully submits that all claims are in condition for allowance, and a Notice of Allowance is respectfully requested in due course.

Statement Of Substance Of The Interview Of June 23, 2006

The Applicant sincerely appreciates all courtesies extended by the Examiner during the telephonic interview of June 28, 2006. In particular, the Applicant appreciates the Examiner's clarification regarding the rejection of Claims 20 and 41 on page 7 of the Office Action mailed June 14, 2006, and that the rejection of Claims 20 an 41 under 35 USC 103(a) should read McCormick in view of Eldridge, not McCormick in view of Kato et al. Accordingly, the Applicant believes that all requirements for a statement of the substance of the interview have been met. If the Examiner should believe that any further submission may be required to satisfy the statement of the substance of the interview, the Applicant respectfully requests that the Examiner contact the Attorney for the Applicant (Scott C. Hatfield) via telephone at (919) 854-1400.

All Objections To The Drawings Have Been Overcome

The Office Action has objected to the drawings stating that the "heat dissipating layer between the first and second electronic substrates" must be shown or the features canceled from the claim(s). As Claims 20, 41, and 53 have been canceled, all objections relating to the heat dissipating layer have been overcome.

All Claim Rejections Under 35 U.S.C. Sec. 112 Have Been Overcome

Claims 19 and 52 have been rejected under 35 U.S.C. Sec. 112, second paragraph. In particular, the Office Action states that the recitation "wherein the signal path is free of electrical coupling with an electronic circuit of the third electronic substrate" inaccurately defines the invention. In order to reduce issues for further consideration, the Applicants have amended Claims 19 and 52 as set forth in the "Listing Of Claims" provided above. According, all rejections under 35 U.S.C. Sec. 112 have been overcome.

Independent Claim 1 Is Patentable Over McCormick

Claim 1 has been rejected under 35 U.S.C. Sec. 102(b) as being anticipated by U.S. Patent No. 6,369,448 to McCormick ("McCormick"). The Applicants respectfully submit, however, that Claim 1 is patentable over McCormick for at least the reasons discussed below. In particular, Claim 1 recites an electronic device comprising:

> a first integrated circuit substrate;
> a second integrated circuit substrate on the first integrated circuit substrate;
> a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates;
> a first electrical and mechanical connection between the first and third integrated circuit substrates wherein the first electrical and mechanical connection bypasses the second integrated circuit substrate;
> a second electrical and mechanical connection between the second and third integrated circuit substrates; and
> a third electrical and mechanical connection between the first and second integrated circuit substrates.

Accordingly, Claim 1 has been amended to clarify that the electronic substrates are integrated circuit substrates, and similar amendments have been made throughout the claims.

In support of the rejection, the Office Action states that: "McCormick discloses in Fig. 4 an electronic device comprising a first 402, second 412 and third 410 electronic substrates." With respect to Figure 4 of McCormick, McCormick discusses a "packaging substrate 402 composed of any suitable material, such as ceramic or polymer/composite materials...." (Underline added.) McCormick, column 6, lines 55-58. Moreover, McCormick states that:

> The substrate 402 has two flip chips electronically connected to it via BGSs: A larger, upper chip 410 overlies a lower, smaller chip 412."

McCormick, col. 7, lines 7-9. Accordingly, McCormick discusses two flip chips 410 and 412 on a packaging substrate 402. McCormick, however, fails to teach or suggest first, second, and third integrated circuit substrates.

Accordingly, the Applicants respectfully submit that Claim 1 is patentable over McCormick. In addition, dependent Claims 2-8, 64-65, and 68 are patentable at least as per the patentability of Claim 1 from which they depend.

Independent Claims 9, 15, And 19 Are Patentable Over Lin

Claims 9, 15, and 19 have been rejected under 35 U.S.C. Sec. 102(e) as being anticipated by U.S. Patent Publication No. 2003/0122240 to Lin ("Lin"). The Applicant respectfully submits that Claims 9, 15, and 19 are patentable over Lin for at least the reasons discussed below. Claim 9, for example, has been amended to recite an electronic device comprising:

> a first integrated circuit substrate;
> a second integrated circuit substrate on the first integrated circuit substrate;
> a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates;
> a first conductive bump between the first and third integrated circuit substrates wherein the first conductive bump is spaced apart from and extends past an edge of the second integrated circuit substrate wherein the first conductive bump provides electrical and mechanical connection between the first and third integrated circuit substrates; and
> a second conductive bump between the second and third integrated circuit substrates wherein the second conductive bump provides electrical and mechanical connection between the second and third integrated circuit substrates;
> wherein each of the first, second, and third integrated circuit substrates includes a device side having electronic circuits thereon and a backside, wherein the device sides of the first, second, and third integrated circuit substrates face a first direction, and the backsides of the first, second, and third integrated circuit substrates face a second direction.

In support of the rejection of Claim 9, the Office Action states that:

> Lin ... discloses an electronic device in Fig. 2A comprising first CH2, second CH3 and third CH4 electronic substrates, a first ... connection BSB between the first and third substrates, and a second ... connection B between the second and third substrates.

Office Action, page 5. In Figure 2A of Lin, however, none of the "big solder balls BSB" is between any of the chips CH1, CH2, CH3, and/or CH4. Accordingly, Lin fails to teach or suggest a first conductive bump between first and third integrated circuit substrates wherein the first conductive bump is spaced apart from and extends past an edge of a second integrated circuit substrate. Moreover, chips CH1, CH2, CH3, and/or CH4 of Figure 2A of Lin alternatingly face in opposite directions. Stated in other words, device sides of chips CH1 and CH3 face up while device sides of chips CH2 and CH4 face down (as indicated by the connections provided through the solder balls B). Accordingly, Lin also fails to teach or suggest device sides of first, second, and third integrated circuit electronic substrates facing a same direction.

Claim 9 is thus patentable over Lin for at least the reasons discussed above. Moreover, Claims 15 and 19 are patentable for reasons similar to those discussed above with respect to Claim 9. In addition, dependent Claims 10-14, 16-18, 62, 66-67, and 69-71 are patentable at least as per the patentability of Claims 9, 15, and 19 from which they depend.

Claim 21 Is Patentable Over Mess And Lin

Claim 21 has been rejected under 35 U.S.C. Sec. 102(e) as being anticipated by U.S. Patent No. 6,900,528 to Mess et al. ("Mess"). Claim 21 has also been rejected under 35 U.S.C. Sec. 103(a) as being unpatentable over Lin in view of Mess. The Applicant respectfully submits that Claim 21 is patentable over Mess and Lin. As amended, Claim 21 recites an electronic device comprising:

> a printed circuit board;
> a first integrated circuit substrate on the printed circuit board;
> a second integrated circuit substrate on the first integrated circuit substrate wherein the first integrated circuit substrate is between the printed circuit board and the second integrated circuit substrate; and
> a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates, wherein the second integrated circuit substrate is offset relative to the first and third integrated circuit substrates so that the first and third integrated circuit substrates extend beyond a first end of the second integrated circuit substrate wherein a second end of the second integrated circuit substrate extends beyond the first and third integrated circuit substrates wherein each of the first, second, and third integrated circuit substrates is on a same side of the printed circuit board and wherein each of the first,

second, and third integrated circuit substrates has a device side facing the printed circuit board and a backside facing away from the printed circuit board.

Each of Lin and Mess teach away from first, second, and third integrated circuit electronic substrates on a same side of a printed circuit board and having device sides facing the same printed circuit board. In Figures 17-23 of Mess, the device sides of the semiconductor die 60A-D (as indicated by bond pads 54A-D) face away from the substrate 70, which may be a circuit board, memory card substrate, or multimedia card substrate (*see*, Mess, col. 6, lines 50-54), or a metallized lead frame (*see*, Mess, col. 9, lines 47-48). In Lin, the chips CH1, CH2, CH3, and CH4 alternatingly face in opposite directions. Accordingly, neither Lin nor Mess, taken alone or in combination, teaches or suggests devices sides of first, second, and third integrated circuit electronic devices facing a same printed circuit board.

Accordingly, the Applicants respectfully submit that Claim 21 is patentable over Lin and Mess for at least the reasons discussed above. The Applicants further submit that new Claim 75 is patentable for reasons similar to those discussed above with respect to Claim 21. In addition, dependent Claims 35-40 and 76-79 are patentable at least as per the patentability of Claims 21 and 75 from which they depend.

Claim 27 Is Patentable Over McCormick

Claim 27 has been rejected under 35 U.S.C. Sec. 102(b) as being anticipated by McCormick. Claim 27, however, is patentable over McCormick for at least the reasons discussed below. As amended, Claim 27 recites an electronic device comprising:

> a printed circuit board;
> a first integrated circuit substrate on the printed circuit board;
> a second integrated circuit substrate on the first integrated circuit substrate wherein the first integrated circuit substrate is between the printed circuit board and the second integrated circuit substrate;
> a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates, wherein the second integrated circuit substrate is offset relative to the first and third integrated circuit substrates so that the first and third integrated circuit substrates extend beyond an end of the second integrated circuit substrate;
> a first conductive bump between the first and third integrated circuit substrates, wherein the first conductive bump provides electrical and mechanical connection between the first and third integrated circuit substrates; and

a second conductive bump between the second and third integrated circuit substrates, wherein the second conductive bump provides electrical and mechanical connection between the second and third integrated circuit substrates;

wherein the first, second, and third integrated circuit substrates have a same size.

The Applicant respectfully submits that McCormick teaches away from a first, second, and third integrated circuit electronic substrates having a same size. In particular, McCormick states that: "A larger, upper chip 410 overlies a lower, smaller chip 412." (Underline added.) McCormick, col. 7, lines 8-9. McCormick also fails to teach or suggest first, second, and third integrated circuit electronic substrates, wherein the second integrated circuit electronic substrate is between the first and third integrated circuit electronic substrates. In contrast, Figure 4 of McCormick shows a packaging substrate 402 and two flip chips 410 and 412.

Accordingly, McCormick fails to teach or suggest the structure of Claim 27, and Claim 27 is thus patentable over McCormick. In addition, dependent Claims 28 and 73 are patentable at least as per the patentability of Claim 27 from which they depend.

Claim 29 Is Patentable Over McCormic, Lin, and Mess

Claim 29 has been rejected under 35 U.S.C. Sec. 102(b) as being anticipated by McCormick, and Claim 29 has also been rejected under 35 U.S.C. Sec. 103(a) as being unpatentable over Lin in view of Mess. Claim 29, however, is patentable over McCormick, Lin, and Mess for at least the reasons discussed below. As amended, Claim 29 recites an electronic device comprising:

a printed circuit board;

a first integrated circuit substrate on the printed circuit board;

a second integrated circuit substrate on the first integrated circuit substrate wherein the first integrated circuit substrate is between the printed circuit board and the second integrated circuit substrate; and

a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates, wherein the second integrated circuit substrate is offset relative to the first and third integrated circuit substrates so that the first and third integrated circuit substrates extend beyond an end of the second integrated circuit substrate;

wherein each of the first, second, and third integrated circuit substrates includes a device side having electronic circuits thereon and a backside, wherein each of the first, second, and third integrated circuit substrates is on a same side of the printed circuit board and wherein the device side of each of the first, second, and third integrated circuit

substrates faces the printed circuit board and the backside of each of the first, second, and third integrated circuit electronic devices faces away from the printed circuit board.

As discussed above with respect to Claim 27, Figure 4 of McCormick shows a structure including a packaging substrate 402 and two flip chips 410 and 412. Accordingly, McCormick fails to teach or suggest first, second, and third integrated circuit electronic substrates as recited in Claim 29.

As discussed above with respect to Claim 21 Lin and Mess teach away from first, second, and third integrated circuit electronic substrates on a same side of a printed circuit board and having device sides facing the same printed circuit board. In Figures 17-23 of Mess, the device sides of the semiconductor die 60A-D (as indicated by bond pads 54A-D) face away from the substrate 70, which may be a circuit board, memory card substrate, or multimedia card substrate (*see*, Mess, col. 6, lines 50-54), or a metallized lead frame (*see*, Mess, col. 9, lines 47-48). In Lin, the chips CH1, CH2, CH3, and CH4 alternatingly face in opposite directions. Accordingly, neither Lin or Mess, taken alone or in combination, teaches or suggests devices sides of first, second, and third integrated circuit electronic devices facing a same printed circuit board.

Accordingly, McCormick, Lin, and Mess fail to teach or suggest the structure of Claim 29, and Claim 29 is thus patentable over the cited art. In addition, dependent Claims 30-31 and 33-34 are patentable at least as per the patentability of Claim 29 from which they depend.

Claim 42 Is Patentable Over

Claim 42 has been rejected under 35 U.S.C. Sec. 102(b) as being anticipated by McCormick, and as being anticipated by Lin, and under 25 U.S.C. Sec. 102(e) as being anticipated by Eldridge. Claim 42, however, is patentable over McCormick, Lin, and Eldridge for at least the reasons discussed below. As amended, Claim 42 recites an electronic device comprising:

> a first integrated circuit substrate having opposing first and second surfaces;
> a second integrated circuit substrate on the first integrated circuit substrate, the second integrated circuit substrate having opposing first and second surfaces;
> a third integrated circuit substrate on the second integrated circuit substrate, the third integrated circuit substrate having opposing first and second surfaces, wherein the

> second integrated circuit substrate is between the first and third integrated circuit substrates, wherein the first surface of the second integrated circuit substrate faces the second surface of the first integrated circuit substrate, and wherein the second surface of the second integrated circuit substrate faces the first surface of the third integrated circuit substrate; and
>
> a signal path extending along a first conductive trace on the first surface of the second integrated circuit substrate, to the second surface of the first integrated circuit substrate, along a second conductive trace on the second surface of the first integrated circuit substrate, to the first surface of the third integrated circuit substrate, along a third conductive trace on the first surface of the third integrated circuit substrate, and to the second surface of the second integrated circuit substrate.

McCormick fails to teach or suggest first, second, and third integrated circuit electronic substrates. As shown in Figure 4 of McCormick, McCormick shows a structure including a packaging substrate 402 and two flip chips 410 and 412. Accordingly, McCormick fails to teach or suggest first, second, and third integrated circuit electronic substrates as recited in Claim 41. McCormick further fails to teach or suggest a second integrated circuit electronic substrate between first and third integrated circuit electronic substrates.

Lin fails to teach or suggest conductive traces on opposing first and second surfaces of an integrated circuit electronic substrate. As shown in Figure 2A of Lin, a single side of each of the chips CH1, CH2, CH3, and CH4 is connected to a printed circuit board PCB2 or PCB3 through solder bumps B. Second sides of the chips CH1, CH2, CH3, and CH4 of Lin are free of electrical connection.

Eldridge also fails to teach or suggest conductive traces on opposing first and second surfaces of an integrated circuit electronic substrate. In support of the rejection, the Office Action states that:

> Eldridge discloses an electronic device comprising at least three electronic substrates 34 or 26 each having on both surfaces "signal path" or traces for electrically connecting each of the substrates.

Office Action, page 7. As shown in Figure 1 of Eldridge, Eldridge discusses a structure including semiconductor devices 24 and stacking substrates 26. The stacking structures 26 of Eldridge, however, are not integrated circuit electronic substrates, and the semiconductor devices 24 of Eldridge do not include conductive traces on opposing first and second surfaces thereof. As shown in Figure 1 of Eldridge, contact pads 34 of stacking substrate 26 couple with

a lower surface of semiconductor device 24, but there is no electrical coupling to an upper surface of semiconductor device 24. Instead, a heat spreader is provided over semiconductor device 24.

Accordingly, McCormick, Lin, and Eldridge fails to teach or suggest the structure of Claim 42, and Claim 42 is thus patentable over the cited art. In addition, dependent Claims 44-51 are patentable at least as per the patentability of Claim 42 from which they depend.

Claim 52 Is Patentable Over Lin

Claim 52 has been rejected under 35 U.S.C. Sec. 102(e) as being anticipated by Lin. Claim 52, however, is patentable over Lin for at least the reasons discussed below. As amended, Claim 52 recites an electronic device comprising:

> a first integrated circuit substrate having opposing first and second surfaces;
> a second integrated circuit substrate on the first integrated circuit substrate, the second integrated circuit substrate having opposing first and second surfaces;
> a third integrated circuit substrate on the second integrated circuit substrate, the third integrated circuit substrate having opposing first and second surfaces, wherein the second integrated circuit substrate is between the first and third integrated circuit substrates;
> a signal path extending along the first surface of the second integrated circuit substrate, to the second surface of the first integrated circuit substrate, along the second surface of the first integrated circuit substrate, to the first surface of the third integrated circuit substrate, along the first surface of the third integrated circuit substrate, and to the second surface of the second integrated circuit substrate; and
> a fourth integrated circuit substrate on the third integrated circuit substrate wherein the third integrated circuit substrate is between the second and fourth integrated circuit substrates; and
> wherein the signal path further extends along the second surface of the second integrated circuit substrate, and to a first surface of the fourth integrated circuit substrate;
> wherein the signal path is electrically coupled directly with an electronic circuit of the fourth integrated circuit substrate, and wherein the signal path is free of direct electrical coupling with any electronic circuit of the second integrated circuit substrate.

The Applicant respectfully submits that Lin fails to teach or suggest a signal path extending along first and second opposing surfaces of a same integrated circuit electronic substrate. As shown in Figure 2A of Lin, each of the chips CH1-CH4 has solder balls on one surface thereof, and the other surface of each of the chips CH1-CH4 is free of solder balls or other electrical connection.

Accordingly, Lin fails to teach or suggest the structure of Claim 52, and Claim 52 is thus patentable over the cited art.

Claim 59 Is Patentable Over Lin

Claim 59 has been rejected under 35 U.S.C. Sec. 102(e) as being anticipated by Lin. Claim 59, however, is patentable over Lin for at least the reasons discussed below. As amended, Claim 59 recites an electronic device comprising:

> a substrate having opposing first and second surfaces;
> a first array of interconnection structures on the first surface of the substrate wherein the first array of interconnection structures are arranged in a first pattern;
> a second array of interconnection structures on the second surface of the substrate wherein the second array of interconnection structures are arranged in a second pattern and wherein the second pattern is a mirror image of the first pattern wherein the substrate comprises an integrated circuit substrate such that the first surface is a device side of the substrate having electronic circuits thereon and the second surface is a backside of the substrate.

Lin fails to teach or suggest an integrated circuit substrate having interconnection structures on opposing surfaces thereof. As shown in Figure 2A of Lin, each of the chips CH1, CH2, CH3, and CH4 has solder bumps B on only one side thereof.

Accordingly, Lin fails to teach or suggest the structure of Claim 59, and Claim 59 is thus patentable over the cited art. In addition, dependent Claims 55-58, 60, 63, and 74 are patentable at least as per the patentability of Claim 59 from which they depend.

CONCLUSION

Accordingly, the Applicants submit that all pending claims in the present application are in condition for allowance, and a Notice of Allowance is respectfully requested in due course. The Examiner is encouraged to contact the undersigned attorney by telephone should any additional issues need to be addressed.

Respectfully submitted,

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Joyce Paoli